CLAIMS:

1. An apparatus for amplitude and phase modulation of a signal comprising:

a reference pulse oscillator arranged to provide a signal in the form of a series of input pulses;

an input for input modulating data including desired amplitude and phase modulation;

a vector logic circuit responsive to the input modulating data;

two digital delay lines each coupled to said reference oscillator and having multiple delay cells for selectively delaying respective pulses of said signal;

two lookup tables each of which contains information for controlling the delay cells of a respective one of the delay lines so that the vector logic circuit controls an overall delay of the respective one of the digital delay lines using the information so as to generate therefrom a component vector which is dependent upon the input modulating data;

two amplitude adjustment circuits each of which contains a switching bank and combiner that enables the summation of input signals from a respective one of the digital delay lines to produce amplitude variances in output vectors therefrom;

and a summer that is coupled to the two amplitude adjustment circuits which combines the output vectors therefrom together.

2. The apparatus according to Claim 1 wherein said vector logic circuit is arranged to utilize the desired magnitude and phase data to determine the required phase and magnitude of the two component vectors.

3. The apparatus according to Claim 2 wherein the vector logic circuit is arranged such that the formula $Cos^{-1}[r/(2V)]$ governs the component vectors angle of rotation away from the desired output phase where, in the governing formula, r represents the desired output magnitude and V is the magnitude of the component vectors.

4. The apparatus according to Claim 2 wherein the vector logic circuit is arranged such that the component vectors have the same magnitude and are equidistant, radially, from the resultant vector.

5. The apparatus according to Claim 2 wherein said vector logic circuit is arranged to compensate for the special cases where the phase of the leading or trailing vectors cross the 360° barrier.

6. The apparatus according to Claim 2 wherein said vector logic circuit is arranged to convert the phase information into an equivalent delay.

7. The apparatus according to Claim 2 wherein said vector logic circuit is arranged to update lookup tables with the information required to reproduce the required delay.

8. The apparatus according to Claim 2 wherein said vector logic circuit is arranged to determine the minimum allowable amplitude of the component vectors required to reproduce the desired resultant vector.

9. The apparatus according to Claim 8 wherein the vector logic circuit is arranged such that the minimum allowable amplitude is larger than or equal to r/2.

10. The apparatus according to Claim 1 wherein each of said delay

lines contains a finite number of sequential or parallel delay cells capable of covering 360° of phase with the desired resolution.

11. The apparatus according to Claim 9 wherein each of said delay cells has equivalent or weighted delay periods.

12. The apparatus according to Claim 10 wherein each of said delay cells contains a feedback edge detector where, upon detection of a falling edge, the delay cell confirms its next status from a lookup table.

13. The apparatus according to Claim 1 wherein each of said digital delay lines contains a finite number of extra delay cells which can be used for compensation for the time resolution steps.

14. The apparatus according to Claim 1 wherein each of said lookup tables contains the delay information required to reproduce a specified phase.

15. The apparatus according to Claim 14 wherein each of said lookup tables is arranged such that it is directly referenced by the digital delay lines in order to control which delay cells are enabled at a given time.

16. The apparatus according to Claim 13 wherein each of said lookup tables contains redundant registers which allow for compensation information.

17. The apparatus according to Claim 1 wherein each of said amplitude adjustment circuits is arranged to provide finite discrete amplitude adjustment to a phase varying signal.

18. The apparatus according to Claim 17 wherein each of said amplitude adjustment circuits is arranged to perform the discrete amplitude

adjustment by the summation of multiple in phase vectors exiting the digital delay line.

19. The apparatus according to Claim 17 wherein each of said amplitude adjustment circuits is controlled by the vector logic circuit

20. The apparatus according to Claim 17 wherein each of said amplitude adjustment circuits is arranged such that each discrete magnitude step is twice the magnitude of the last increment.

21. The apparatus according to Claim 1 wherein said summer is coupled to the two amplitude adjustment circuits for the purpose of combining two variable phase and amplitude component vectors into a resultant vector containing a desired amplitude and phase.

22. The apparatus according to Claim 1 wherein said reference pulses are a high power pulse train, with the pulses being at least as large as the desired output power of the modulated signal.

23. The apparatus according to Claim 1 in which the input for said input modulating data is digital such that digital data is converted into the output vector which is an analog signal, without the use of digital to analog converters.

24. The apparatus according to Claim 1 in which the input for said input modulating data is digital such that digital data is converted into the output vector which is an analog signal, and wherein the output vector is transmitted with minimal amplification.